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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,727	08/04/2003	Robert O. Conn	X-1415 US	5587

24309 7590 08/18/2005

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EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,727	CONN ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-13 and 15-21* is/are rejected.

7)☒ Claim(s) *6-8 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: pages 8, 11 and 17 are not aligned.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5, 13, 15, 16 and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Ogawa et al. (USP 5,835,045).

Figure 9 of Ogawa et al. shows a multiplexer comprising a first data input lead (IN.1), a second data input lead (IN.2), a data output lead (OUT), the multiplexer comprising a plurality of series capacitor coupling structures (405, 410-1; 405, 410-2; 405, 410-n), each series capacitor coupling having an input lead (IN.1, IN.2, IN.N), a control lead (414), an output lead ((b)), wherein the input lead is capacitively coupled to the output lead when the control lead is floating, and wherein the input lead is decoupled from the output lead when the control lead is driven with a DC voltage, wherein the input lead of a first of the SCC structures is the input data input lead of the multiplexer, and wherein the input lead of a second of the SCC structures is the second data input lead of the multiplexer, and wherein the output lead of the first SCC structure is coupled to the output lead of the second SCC structure and an output latch (510, 511, 508, 509)

having an input lead and an output lead, the input lead of the output latch being coupled to the output lead of the first SCC structure, the output lead of the output latch being the data output lead of the multiplexer as called for in claims 1, 13 and 20.

Regarding claim 2, when the control signal (414) at a low level (ground) the switch 405 is decoupled from the output lead ((b)).

Regarding claims 3, 15 and 21, figure 9 show one bit of digital information (ΦRES) being stored in a memory cell (not shown).

Regarding claim 5, figure 9 shows an output latch having an amplifier portion (404, 501-504) and a latch portion (508-511).

Regarding claim 16, the intervening node ((b)) is biasing with a bias voltage (404 via the means 501 and 502).

4. Claims 1-5, 11-13, 15, 16, 19 and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (USP 5,410,192).

Figure 23 of Yamada shows a multiplexer comprising a first data input lead (Va), a second data input lead (Vb), a data output lead (15Q), the multiplexer comprising a plurality of series capacitor coupling structures (105a, 105Qc; 105b, 105Qc), each series capacitor coupling having an input lead (Va, Vb), a control lead (N1a, N1b), an output lead (N3), wherein the input lead is capacitively coupled to the output lead when the control lead is floating, and wherein the input lead is decoupled from the output lead when the control lead is driven with a DC voltage, wherein the input lead of a first of the SCC structures is the input data input lead of the multiplexer, and wherein the input lead of a second of the SCC structures is the second data input lead of the multiplexer, and wherein the output lead of the first SCC structure is coupled to the

output lead of the second SCC structure and an output latch (86, 83) having input lead and an output lead, the input lead of the output latch being coupled to the output lead of the first SCC structure, the output lead of the output latch being the data output lead of the multiplexer as called for in claims 1, 12-13 and 19-20.

Regarding claim 2, when the control signal (N1b) at a low level (ground) the switch 105a3is decoupled from the output lead.

Regarding claims 3-4, 15 and 21, figure 23 show one bit of digital information (Da1, Db1) being stored in a memory cell (11).

Regarding claim 5, figure 23 shows an output latch having an amplifier portion (81, 16a, 16b) and a latch portion (82, 83).

Regarding claim 11, the multiplexer is a two to one multiplexer that is a part of a larger multiplexer 4 to 1, wherein the larger multiplexer includes SCC structures in addition to the first and second SCC structures that are part of the two to one multiplexer.

Regarding claim 16, the intervening node (N3) is biasing with a bias voltage (vdd via the means 105e1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-10 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Ogawa (USP 5,835,045). Figure 9 of Ogawa et al. shows a multiplexer comprising a first data input lead (IN.1), a second data input lead (IN.2), a data output lead (OUT), the multiplexer comprising a plurality of series capacitor coupling structures (405, 410-1; 405, 410-2; 405, 410-n), each series capacitor coupling having an input lead (IN.1, IN.2, IN.N), a control lead (414), an output lead ((b)), wherein the input lead is capacitively coupled to the output lead when the control lead is floating, and wherein the input lead is decoupled from the output lead when the control lead is driven with a DC voltage, wherein the input lead of a first of the SCC structures is the input data input lead of the multiplexer, and wherein the input lead of a second of the SCC structures is the second data input lead of the multiplexer, and wherein the output lead of the first SCC structure is coupled to the output lead of the second SCC structure and an output latch (510, 511, 508, 509) having an input lead and an output lead, the input lead of the output latch being coupled to the output lead of the first SCC structure, the output lead of the output latch being the data output lead of the multiplexer.

What not shown in Ogawa is having the circuit in a programmable logic device or gate array as called for in claims 9, 10, 17 and 18. However, it is known in the art that programmable logic device (PLD) can be mass produced and it is very economical. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to mass produced the circuit in a PLD structure for the purpose of saving cost.

Claims 9-10 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (USP 5,410,192). Figure 23 of Yamada shows a multiplexer comprising a first data input lead (Va), a second data input lead (Vb), a data output lead (15Q), the multiplexer

comprising a plurality of series capacitor coupling structures (105a, 105Qc; 105b, 105Qc), each series capacitor coupling having an input lead (Va, Vb), a control lead (N1a, N1b), an output lead (N3), wherein the input lead is capacitively coupled to the output lead when the control lead is floating, and wherein the input lead is decoupled from the output lead when the control lead is driven with a DC voltage, wherein the input lead of a first of the SCC structures is the input data input lead of the multiplexer, and wherein the input lead of a second of the SCC structures is the second data input lead of the multiplexer, and wherein the output lead of the first SCC structure is coupled to the output lead of the second SCC structure and an output latch (86, 83) having input lead and an output lead, the input lead of the output latch being coupled to the output lead of the first SCC structure, the output lead of the output latch being the data output lead of the multiplexer.

What not shown in Yamada is having the circuit in a programmable logic device or gate array as called for in claims 9, 10, 17 and 18. However, it is known in the art that programmable logic device (PLD) can be mass produced and it is very economical. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to mass produced the circuit in a PLD structure for the purpose of saving cost.

Allowable Subject Matter

6. Claims 6-8, and14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

7/26/2005